

UPPER MEMORY TEST 1

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UPPER MEMORY TEST 1

ORG 10100 / UPPER MEM TEST

100	004001	S LAW 1
101	020143	DAC #TWD
102	060143	S1 LAC #TWD
103	003001	RAL 1
104	020143	DAC #TWD
105	104001	LWC 1
106	020010	DAC 10010
107	060143	LAC #TWD
110	120010	I DAC 10010
111	100002	CMA
112	120010	I DAC 10010
113	060153	LAC =7771
114	074010	SAM 10010
115	010107	JMP .-6
116	104001	LWC 1
117	020010	DAC 10010
120	060143	LAC #TWD
121	174010	I SAM 10010
122	034132	JMS E
123	100002	CMA
124	174010	I SAM 10010
125	034132	JMS E
126	060153	LAC =7771
127	074010	SAM 10010
130	010120	JMP .-10
131	010102	JMP S1
		E BSS 1
133	020144	DAC #SAV
134	060010	LAC 10010
135	000000	HLT
136	020145	DAC #TMP
137	160145	I LAC #TMP
140	000000	HLT
141	060144	LAC #SAV
142	110132	I JMP E
		S2 REL .+20
163	104001	P LWC 1 / TEST MEM SIZE
164	124154	I XAM =7776
165	020146	DAC #SVA
166	060154	LAC =7776
167	020147	DAC #SVB
170	020150	DAC #SVE
171	060147	LAC #SVB
172	064155	ADD =10000
173	020147	DAC #SVB
174	100001	CLA
175	124147	I XAM #SVB
176	020151	DAC #SVC
177	160150	I LAC #SVE
200	102002	ASM
201	010205	JMP .+4
202	060151	LAC #SVC
203	120147	I DAC #SVB

test 0 → 7770

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204 010171 JMP .-13
205 060146 LAC #SVA
206 120154 I DAC =7776
207 060147 LAC #SVB
210 070156 SUB =10006
211 020152 DAC #BLM
212 010100 JMP S
REL 37714
7714 013400 JMP 37400
REL 37400
7400 001052 HOF
7401 113402 I JMP .+1
7402 010163 ZRO P
REL S2
END

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153 007771
154 007776
155 010000
156 010006

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SYM
E 132
P 163
S 100
S1 102
S2 143

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UNU SYM

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```

ERR

```

```

SAV
143 TWD
144 SAV
145 TMP
146 SVA
147 SVB
150 SVE
151 SVC
152 BLM

```

```

LIT
153 007771
154 007776
155 010000
156 010006

```

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MAC

```

```

ORG 100
END 142
LAS 156

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