

LOWER MEMORY TEST 1

3600-3677

LOWER MEMORY TEST 1

ORG 100 / LOWER MEM TEST

100 004001 S LAW 1
 101 020143 DAC #TWD
 102 060143 S1 LAC #TWD
 103 003001 RAL 1
 104 020143 DAC #TWD
 105 004200 LAW 200
 106 020010 DAC 10
 107 060143 LAC #TWD
 110 120010 I DAC 10
 111 100002 CMA
 112 120010 I DAC 10
 113 060144 LAC #BLM
 114 074010 SAM 10
 115 010107 JMP •-6
 116 004200 LAW 200
 117 020010 DAC 10
 120 060143 LAC #TWD
 121 174010 I SAM 10
 122 034132 JMS E
 123 100002 CMA
 124 174010 I SAM 10
 125 034132 JMS E
 126 060144 LAC #BLM
 127 074010 SAM 10
 130 010120 JMP •-10
 131 010102 JMP S1

E BSS 1

133 020145 DAC #SAV
 134 060010 LAC 10
 135 000000 HLT
 136 020146 DAC #TMP
 137 160146 I LAC #TMP
 140 000000 HLT
 141 060145 LAC #SAV
 142 110132 I JMP E

S2 REL •+20

P LMC 1 / TEST MEM SIZE

163 104001 I XAM =7776
 164 124153 I XAM =7776
 165 020147 DAC #SVA
 166 060153 LAC =7776
 167 020150 DAC #SVB
 170 020151 DAC #SVE
 171 060150 LAC #SVB
 172 064154 ADD =10000
 173 020150 DAC #SVB
 174 100001 CLA
 175 124150 I XAM #SVB
 176 020152 DAC #SVC
 177 160151 I LAC #SVE
 200 102002 AS4
 201 010205 JMP •+4
 202 060152 LAC #SVC

Some kind of state of machine
pass of 200 (skips normal program)
200 → (BLM)
(out bit)

address in error
content of address

PROD

```

203 120150 I DAC #SVB
204 010171 JMP .-13
205 060147 LAC #SVA
206 120153 I DAC =7776
207 060150 LAC #SVB
210 070155 SUB =10006
211 020144 DAC #BLM
212 010100 JMP S
REL 37714
7714 013400 JMP 37400
REL 37400
7400 001052 HOF
7401 113402 I JMP .+1
7402 000163 ZRO P
REL S2
END

153 007776
154 010000
155 010006

```

SYM

```

E 132
P 163
S 100
S1 102
S2 143

```

UNU SYM

ERR

SAV

```

143 TWD
144 BLM
145 SAV
146 TMP
147 SVA
150 SVB
151 SVE
152 SVC

```

LIT

```

153 007776
154 010000
155 010006

```

MAC

```

ORG 100
END 142
LAS 155

```